REMARKS

I. Status Summary

Claims 1-3 are pending in the present application. Claims 1-3 have been amended. Therefore, upon entry of this Amendment, Claims 1-3 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

Support for the paragraph inserted after line 6 of page 2, of the present application, can be found on page 2 of the **Amended Sheets** included with the present application. The **Amended Sheets** were previously filed by Applicants as an amendment to PCT International Application No. PCT/EP00/09267, which is related to the present application.

Claim 1 has been amended to place the claim in better method claim format.

Support for the features added to Claims 1 and 3 can be found throughout the present application, particularly at page 3, lines 1-4, page 14, lines 20-35, and page 16, lines 36-39.

II. Specification

The disclosure stands objected to because of various informalities. The Examiner stated that the disclosure contains the following errors: misspelling of the word "hazard" at pages 1, 5, 7, and 10; English grammar error at page 2a; and, with the deletion on page 2, the remaining sentence between pages 1 and 2 is

grammatically incorrect. (Official Action, page 2.) The disclosure has been amended as suggested by the Examiner.

The Examiner stated that the title is not descriptive. In particular, the Examiner stated that a new title is required that is clearly indicative of the invention to which the claims are directed. (Official Action, page 2.) The title has been amended to "Method and Apparatus for Processing Conditional Jump Instructions By Means of Pre-Conditions and Post-Conditions in a Processor with Pipelined Architecture". Applicant respectfully submits that the new title is descriptive.

For the above reasons, applicant respectfully submits that the objection of the disclosure should be withdrawn.

III. Claim Rejections Under 35 U.S.C. § 112

Claims 1-3 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner stated that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to make or use the invention. (Official Action, page 3.) Regarding Claims 1-3, the Examiner contends that it is unclear how the precondition and post-condition bits (P1 and Q1) are implemented. (Official Action, page 3.) More particularly, the Examiner stated "applicant states an instruction 'ADD R1, R2, #JMP, ON ZERO,' then says it is extended to 'P1 ADD R1, R2, #JMP, Q1" at page 7 of the present application. (Official Action, page 3.) Further, the Examiner stated that it is unclear what happened to the previously stated "ON ZERO". (Official Action, page 3.) Regarding the first instruction "ADD R1, R2, #JMP, ON ZERO" at

page 7 of the present application, the conditional jump is executed if R1 is zero. This condition is specified by the flag "ON ZERO". Further, regarding the instruction "P1 ADD R1, R2, #JMP, Q1", applicant submits that this instruction the post-condition Q1 is only a generalized representation of this condition. Support for this assertion is provided at page 7, lines 35-37, which reads "Q1 means, execute jump by JMP if Q1 is fulfilled after the calculation of R1 = R1 + R2". Therefore, applicant respectfully submits that the disclosure provides a clear description of the association between the flag "ON ZERO" of the first instruction and the post-condition Q1 of the second instruction.

Regarding sections 10-12 at pages 3-5, of the Official Action, the Examiner stated that page 8, lines 10-15, and page 9, line 1, to page 10, line 2, of the specification are unclear. By the above amendments, applicant has canceled these portions of the disclosure. For this reason, applicant respectfully submits that the rejection due to these portions of the disclosure is moot.

In section 13 at page 5, of the Official Action, the Examiner stated that one of ordinary skill in the art is prevented from understanding the precondition and post-condition concepts in the conditional jump instruction. Further, the Examiner stated that there is no example of a conditional jump instruction with a precondition, post-condition, and jump address as claimed. (Official Action, page 5.) Applicant respectfully submits that the examples provided by Figures 2 and 3 and corresponding description of the present application sufficiently describe an instruction format including a conditional jump instruction with a precondition, a post-condition, and a jump address. For example, referring to Figure 2 of the present application, an

instruction format including a pre-bit, a post-bit, and eight displacement bits is shown. The pre-bit represents a precondition, the post-bit represents a post-condition, and the eight displacement bits represent a jump address. Further, for example, Figure 3 of the present application shows an instruction format including two bits for Q1 (i.e., post-condition), two bits for P1 (i.e., precondition), and eight bits for #JMP (i.e., jump address). Therefore, the disclosure provides at least two examples of an instruction format including a precondition, a post-condition, and a jump address.

For the above reasons, applicant respectfully submits that the specification provides a description sufficient for one of ordinary skill in the art to make and use the subject matter recited by Claims 1-3. Accordingly, applicant respectfully requests that the rejection of Claims 1-3 under 35 U.S.C. § 112, first paragraph, should be withdrawn.

IV. Claim Rejections Under 35 U.S.C. § 103

Claims 1-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mahon et al., "Hewlett-Packard Precision Architecture: The Processor" (hereinafter, "Mahon") in view of Mahlke et al. (hereinafter, "Mahlke"). This rejection is respectfully traversed.

Claim 1 recites a method for processing conditional jump instructions in a processor with pipeline computer architecture. Further, Claim 1 recites loading a decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, and a post-condition. Claim 1 has been amended to recite that the precondition specifies under which conditions the

instruction is actually to be executed. Further, Claim 1 has been amended to recite that the post-condition specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked. Claim 1 also recites execution of the decoded processor instruction if the precondition is fulfilled. Claim 1 has also been amended to recite jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set. Summarily, neither Mahon nor Mahlke, alone or in combination, teaches or suggests each and every feature recited by amended Claim 1.

In contrast, Mahon describes an architecture in which two instructions are combined into one instruction for achieving code compaction, reduction of execution time, and elimination of condition code flip-flops in the processor state. (Mahon, page 10, right column, paragraph 6.) Therefore, each conditional branch instruction includes a data transformation operation, which generates a condition that is used immediately to determine whether the branch is taken or not. An important disadvantage of this procedure described by Mahon is that the data transformation operation for generating the condition has to be performed. Such a data transformation operation results in significant loss of power and cycle time. The loss of power and cycle time is undesirable for a processor with pipelined architectures. In contrast, the post-condition recited by Claim 1 specifies that flag bits of an arithmetic-logic unit are to be checked. Thus, by means of the post-condition recited by Claim 1, only existing resources (i.e., flag bits) of the processor are utilized. This feature can

conserve power and time. There is no disclosure or suggestion in Mahon of checking flag bits, as required by Claim 1.

Mahlke fails to overcome the significant shortcomings of Mahon. The Examiner stated that Mahlke teaches a precondition as recited by Claim 1. (Official Action, pages 6 and 7.) However, Mahlke fails to teach or suggest a post-condition which specifies that a conditional jump is to be processed and the corresponding flag bits of the arithmetic-logic unit are to be checked. Therefore, neither Mahon nor Mahlke, along or in combination, teaches or suggests a post-condition as required by Claim 1. For this reason, applicant respectfully submits that that Claim 1 is not obvious in view of Mahon and Mahlke. Applicant, therefore, respectfully requests that the rejection of Claim 1 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Claim 2 depends from Claim 1, and therefore Claim 2 includes the features of Claim 1. Therefore, Claim 2 is believed to be patentable over Mahon and Mahlke for the same reasons provided for Claim 1. Accordingly, applicant respectfully requests that the rejection of Claim 2 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Claim 3 recites an apparatus for processing conditional jump instructions in a processor with pipeline computer architecture. Further, Claim 3 recites an instruction decoder for decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, and a post-condition. Claim 3 has been amended to recite that the precondition specifies under which conditions the instruction is actually to be executed. Further, Claim 3 has been amended to recite that the post-condition specifies that a conditional jump is to be

processed and the corresponding flag bits of the arithmetic-logic unit are to be checked. Claim 3 has also been amended to recite that the instruction decoder is operable to check, in the case of a fulfilled precondition, whether the post-condition is fulfilled and the flag bits are set, if positive, driving a program counter for forming a jump address as a function of the relative jump distance contained in the processor instruction. Summarily, neither Mahon and Mahlke, alone or in combination, teaches or suggests each and every feature recited by Claim 3.

Similar to Claim 1, Claim 3 recites an instruction decoder for decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, and a post-condition. Further, similar to Claim 1, Claim 3 recites that the precondition specifies under which conditions the instruction is actually to be executed. In addition, similar to Claim 1, Claim 3 recites that the post-condition specifies that a conditional jump is to be processed and the corresponding flag bits of the an arithmetic logic unit are to be checked. For the reasons provided above, Mahon and Mahlke fail to teach or suggest these features. Therefore, applicant respectfully submits that that Claim 3 is not obvious in view of Mom Mahon and Mahlke. Applicant, therefore, respectfully requests that the rejection of Claim 3 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Serial No.: 10/088,988

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.

Date: July 14, 2006

By: Richard E. Jenkins

Richard E. Jenkins
Registration No. 28,428
Customer No: 25297

REJ/BJO/

1406/52